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FPGAs in Software Defined Radio: Past, Present and Future

A personal story

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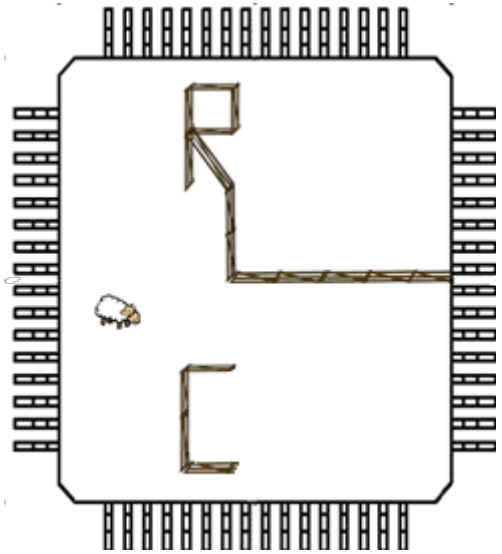
What is New Zealand known for?

What is a reconfigurable gate array?



http://www.coe.neu.edu/Research/rcl/publications/sheepyards.pdf

Early history of Xilinx FPGAs

- The XC2064 introduced in 1985
  - 64 configurable logic blocks (CLBs), with two three-input lookup tables per CLB
- The Xilinx 3000 series introduced in the late 1980s
- Xilinx Virtex-II Pro introduced in 2002
  - The first FPGA with embedded hardcore processing

Xilinx FPGA Devices

Technology	Low-cost	High-performance
120/150 nm		Virtex II, II Pro
90 nm	Spartan 3	Virtex 4
65 nm		Virtex 5
45 nm	Spartan 6	
40 nm		Virtex 6

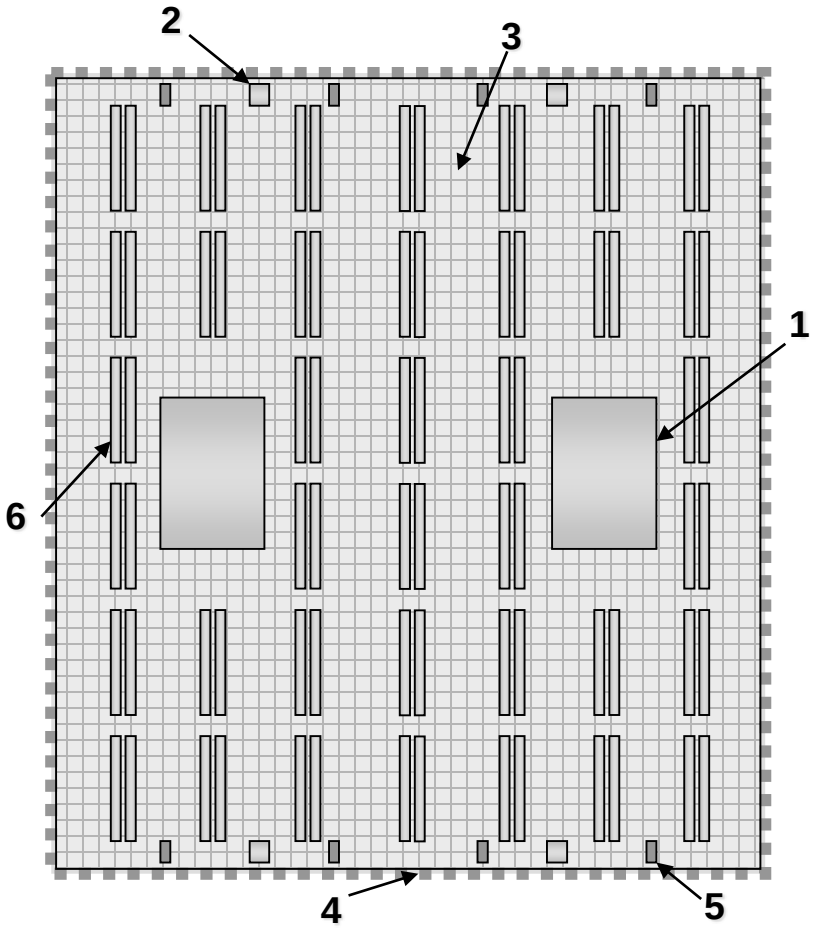
Virtex-II Pro Architecture

First FPGA with embedded hard cores

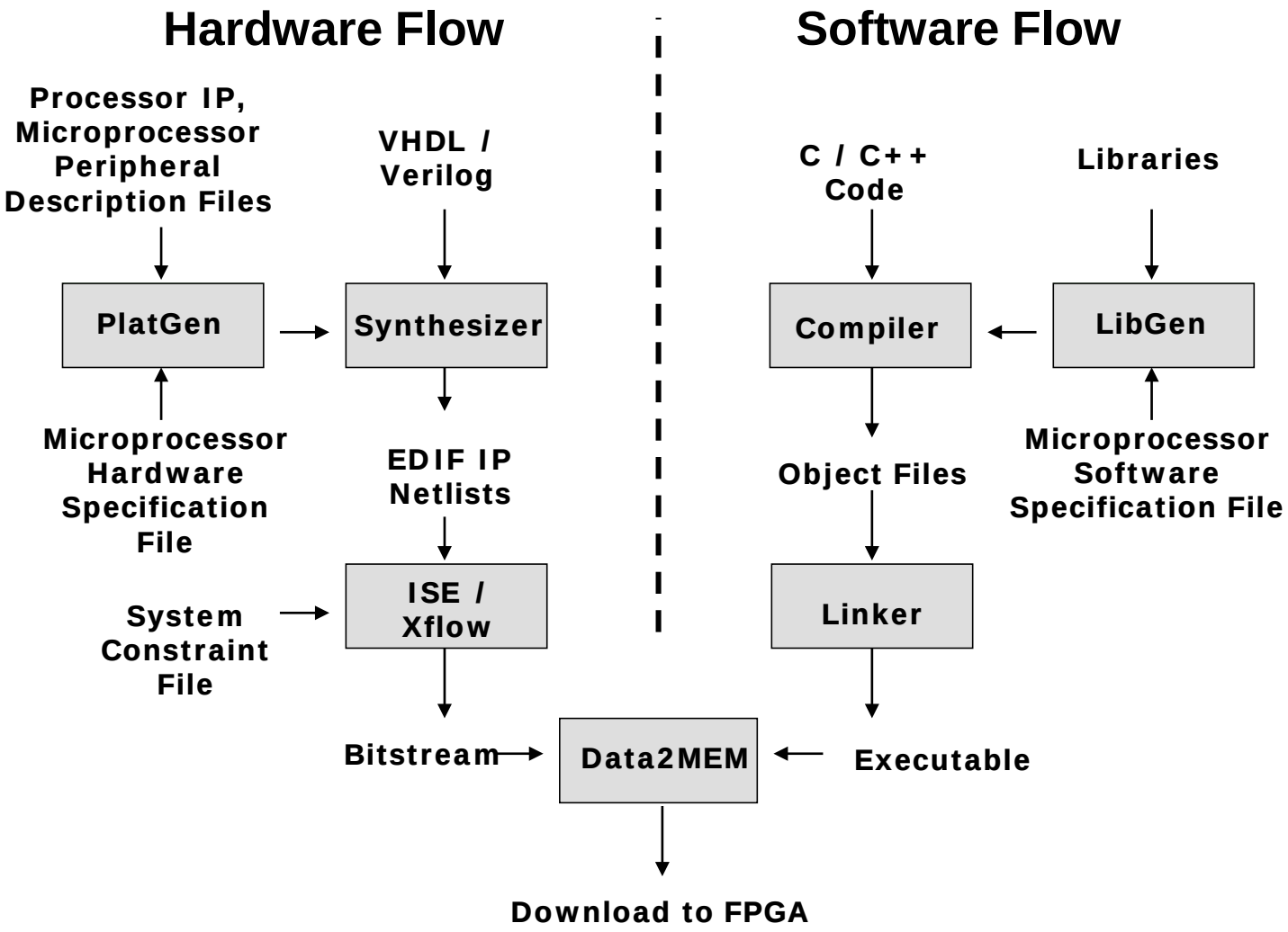
Introduced in 2002

Features:

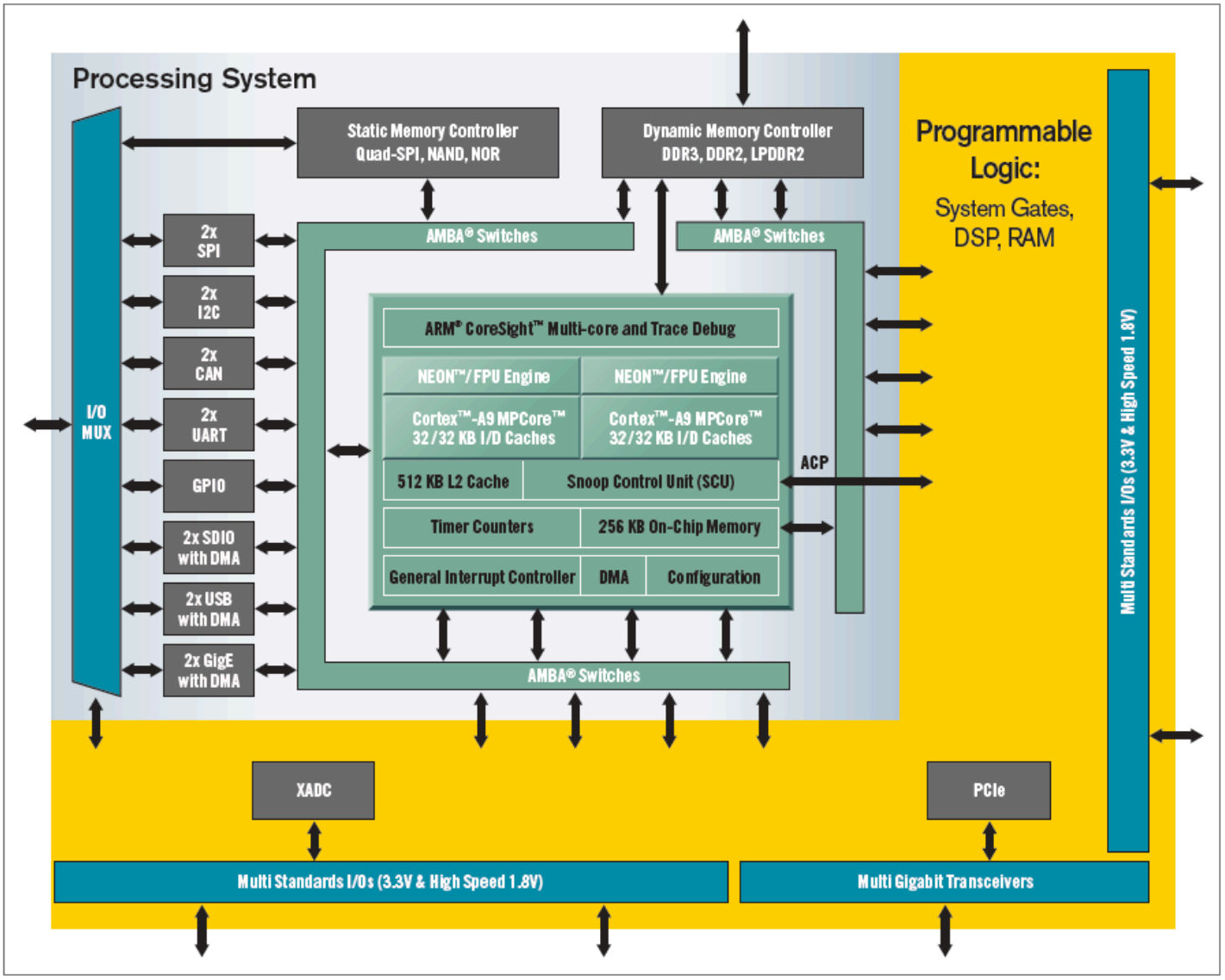
1. Processor Block: PowerPC
2. RocketIO Multi-Gigabit Transceivers
3. CLB and Configurable Logic
4. SelectIO-Ultra
5. Digital Clock Managers
6. Multipliers and Block SelectRAM



Embedded Development Kit (EDK)



Zynq – Zynq 7000



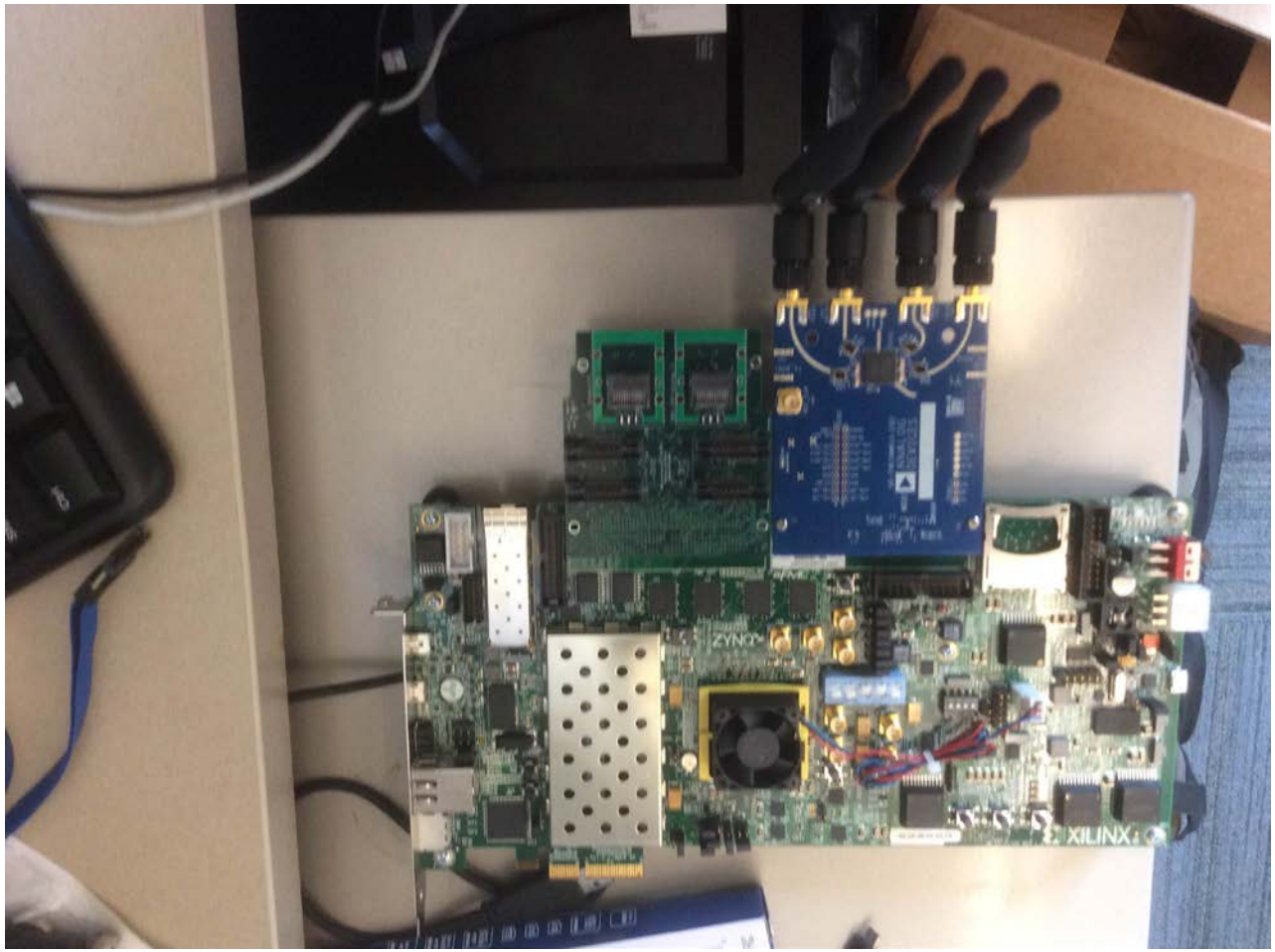
www.xilinx.com

What does this have to do with Software Defined/Cognitive Radio?

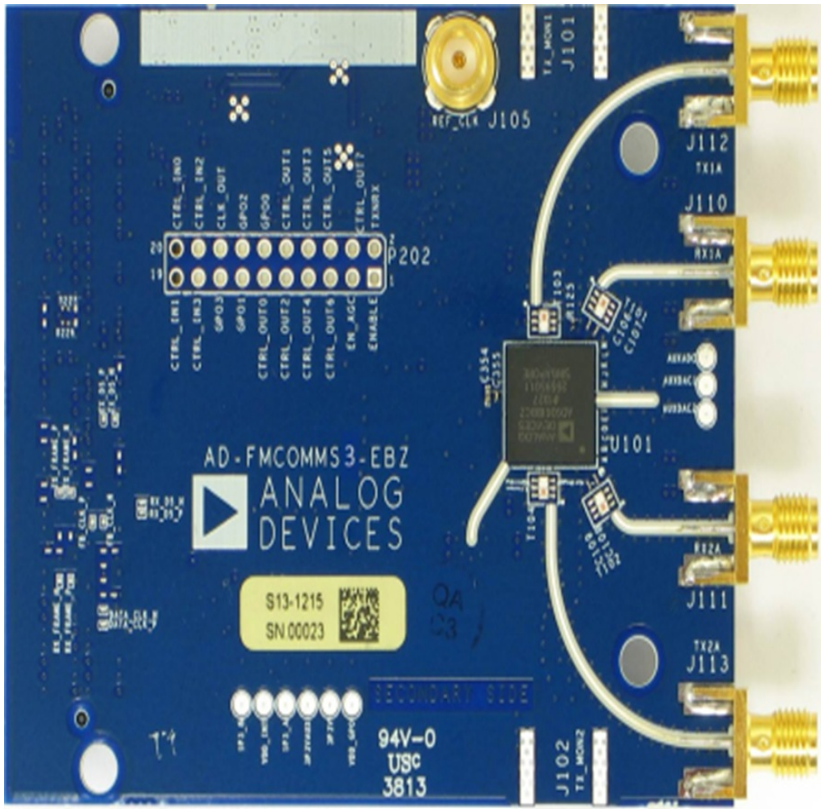
- Past projects:
  - CRUSH: Cognitive Radio Universal Software Hardware
  - CRASH: Cognitive Radio Accelerated with Software and Hardware

- Our current project
  - which still needs a name
  - We ran out of vowels

Current Hardware Platform



ADI FMCOMMS3 Board Overview



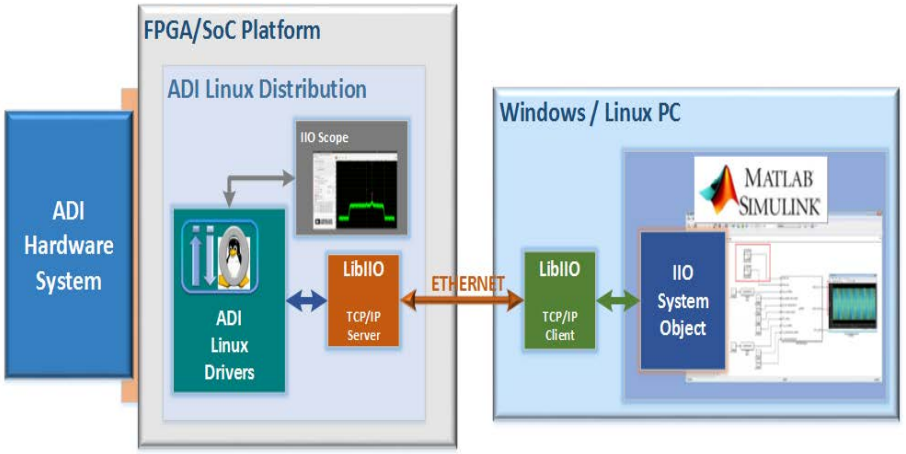
- ADI has FMCOMMS 2/3/4/5
- FMCOMMS 3 operates over a wide tuning range:

  70 MHz – 6 GHz
- 4 antennas:
  - 2x2 MIMO

wiki.analog.com/resources/eval/user-guides/ad-fmcomms3-ebz

ADI RFCOMMS front end

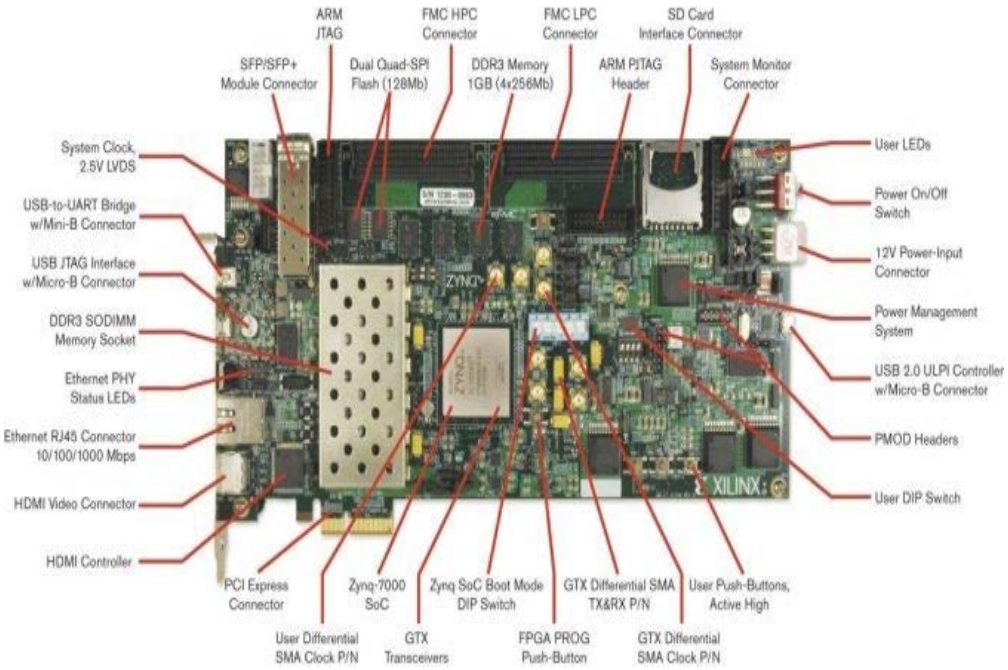
- ADI FMCOMMS3
  - An FMC: FPGA Mezzanine Card
  - Connects to the Xilinx ZC706 or Zedboard
  - LibIIO: ADI library to ease SW development
  - Interfaces with Linux Industrial Input/Output (IIO) devices
  - With MATLAB, you can use an ***IIO System object***
    - Designed to exchange data over Ethernet with an ADI hardware system connected to an FPGA/SoC platform running the ADI Linux distribution



http://wiki.analog.com/resources/tools-software/linux-software/libiio

Xilinx Zynq-7000 Series ZC706 SoC Overview

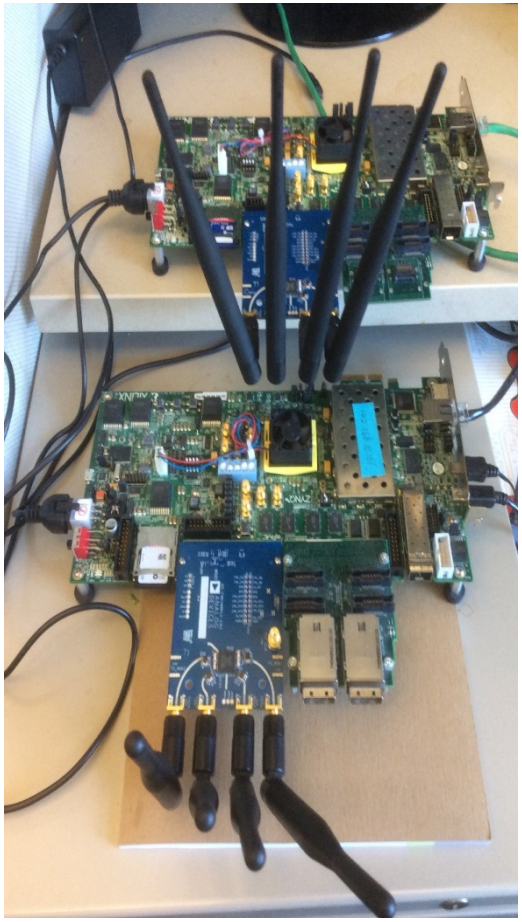
- SoC: System-on-Chip: an ASIC (Application-Specific Integrated Circuit) that can include:
  - Digital, analog, and RF (radio frequency) components
  - Mixed-signal blocks for implementing ADC's/DAC's
- Zynq APSoC (All-Programmable SoC) comprises:
  - Processing System (PS)
  - Programmable Logic (PL)
  - Integrated memory, peripherals, and high-speed communications



http://www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html#hardware

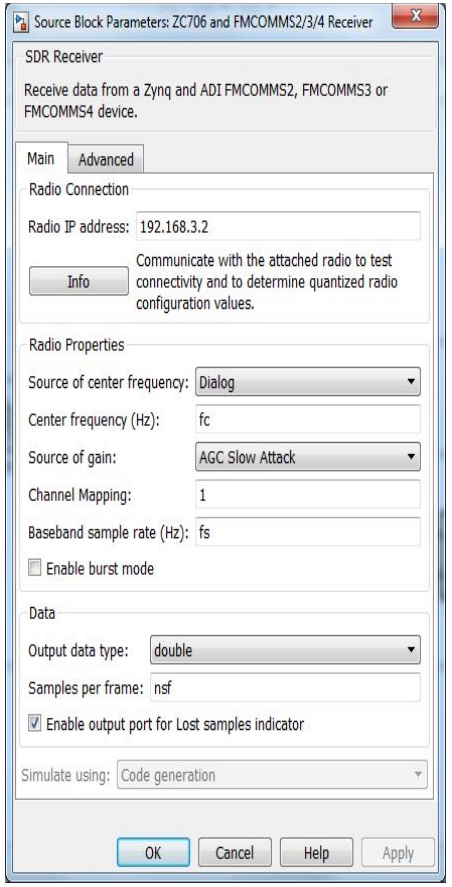
Zynq + FMCOMMS3 Configuration

- Given:
  - Two systems running as Tx and RX
- Challenges:
  - How to partition transceiver subsystem blocks between the Zynq PL & PS?
  - Which tools to use to generate HDL and build an image file for the Zynq?
  - Which tools to use to generate and build C code targeted for the PS ARM?



Current tool support: MathWorks Products

- ***Communications System Toolbox*** *Support Package for Xilinx Zynq-Based Radio*: allows access to RFCOMMS board on Zynq using MATLAB System objects or Simulink blocks
  - Requires Communications System Toolbox, DSP System Toolbox, & Signal Processing Toolbox
- ***HDL Coder Support Package for Xilinx Zynq-7000*** *Platform*: allows generation of HDL from Simulink blocks and placement on the Zynq PL.
  - Requires HDL Coder
- ***Embedded Coder Support Package for Xilinx Zynq-7000 Platform***: allows generation of C code from MATLAB code or Simulink blocks to be built on the Zynq PS's ARM processor.
  - Requires Embedded Coder, Simulink Coder, & MATLAB Coder



"Targeting HDL Optimized QPSK Receiver with Analog Devices FMCOMMS2/3/4."
http://www.mathworks.com/help/releases/R2015a/supportpkg/xilinxzynqbasedradio/examples/targeting-hdl-optimized-qpsk-receiver-with-analog-devices-fmcomms2-3-4.html

Using MathWorks Products

- Benefits:
  - Many blocks for DSP (e.g. FFT & IFFT) and communications (e.g. B/QPSK modulation) support automatic generation of HDL and C code
  - Easy generation of HDL and PL image using HDL Workflow Advisor
  - Communicate between PS & PL via AXI interconnect
- Disadvantages:
  - Not all blocks supported for HDL generation (e.g. correlation)
  - FPGA hardware is sample based, C code is frame based

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HW & SW Joint Modeling Environment: Testbed Requirements

What Does a HW-SW Modeling Environment Need?

1. Reusability: Adapt to Modern Wireless Standards
2. Hardware (HW) Components
3. Software (SW) Tools
4. Model HW-SW Divide for Wireless Behaviors
5. HW-SW Interfacing

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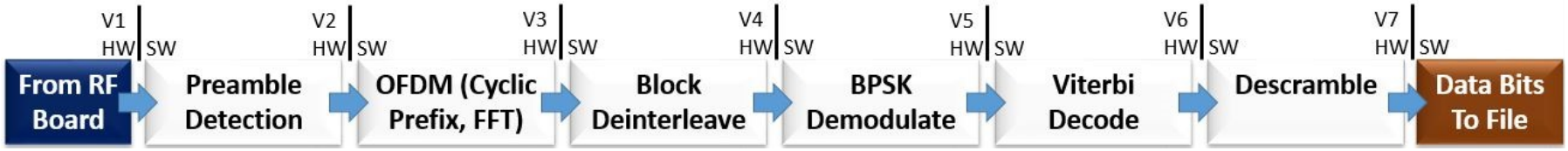
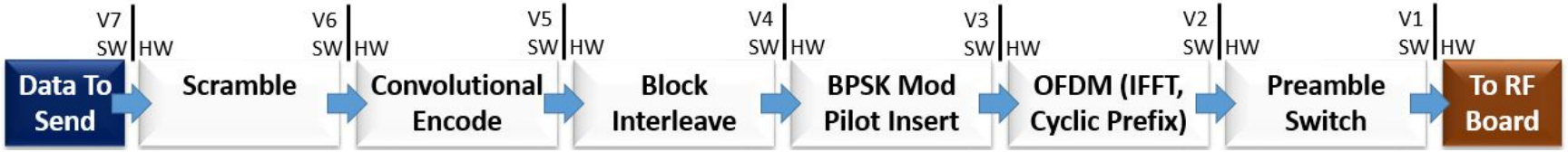
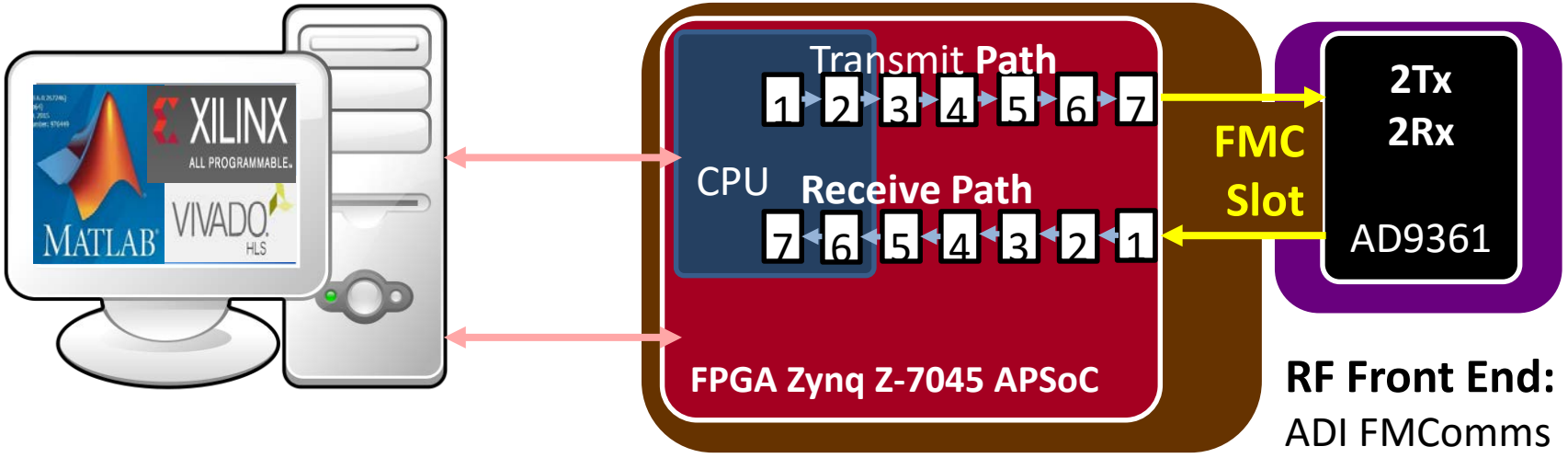
Example 802.11a
Receive and Transmit Hardware Chains





Hardware Components

- Heterogeneous Computing System
- Radio Frequency (RF) Front End
- Host Personal Computer (PC)

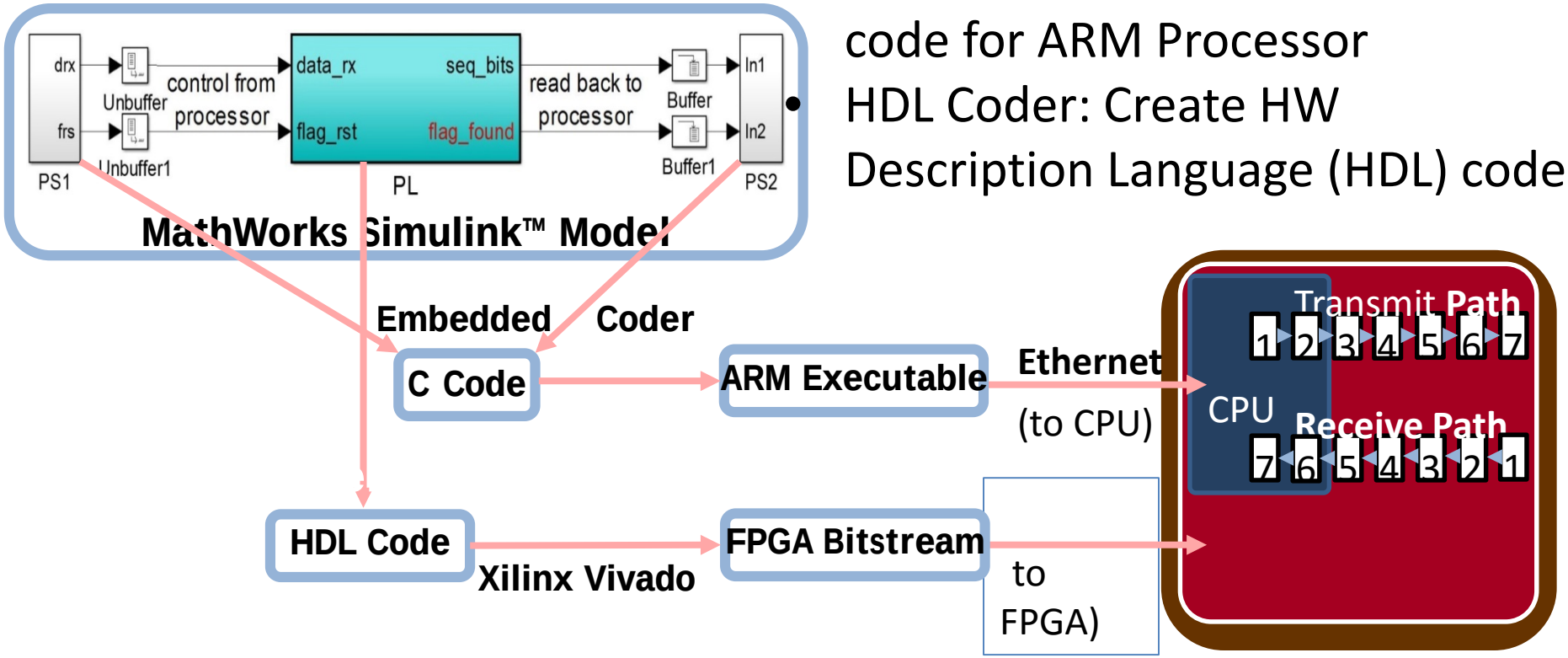


Host PC: Runs SW Tools

Heterogeneous Computing System

Software Tools

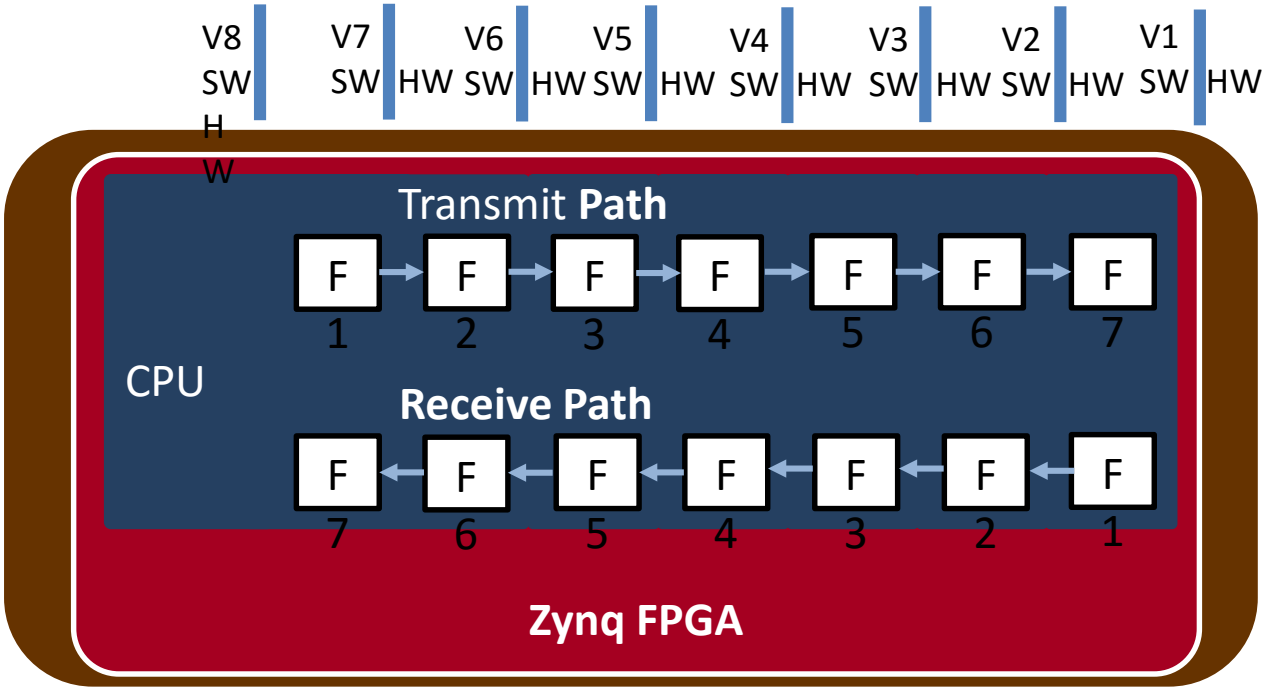
- Simulink: Design Synchronous Dataflow (SDF) Models
- Embedded Coder: Generate C code for ARM Processor
- HDL Coder: Create HW Description Language (HDL) code



Host PC: Runs SW Tools

Zynq Z-7045 APSoC

Behaviors



Heterogeneous Computing System

- **V1: SW-only model**
- V2: Adds Tx F7 & Rx F1 to HW
- V3: Adds Tx F6 & Rx F2 to HW
- V4: Adds Tx F5 & Rx F3 to HW
- V5: Adds Tx F4 & Rx F4 to HW
- V6: Adds Tx F3 & Rx F5 to HW
- V7: Adds Tx F2 & Rx F6 to HW
- V8: HW-only model

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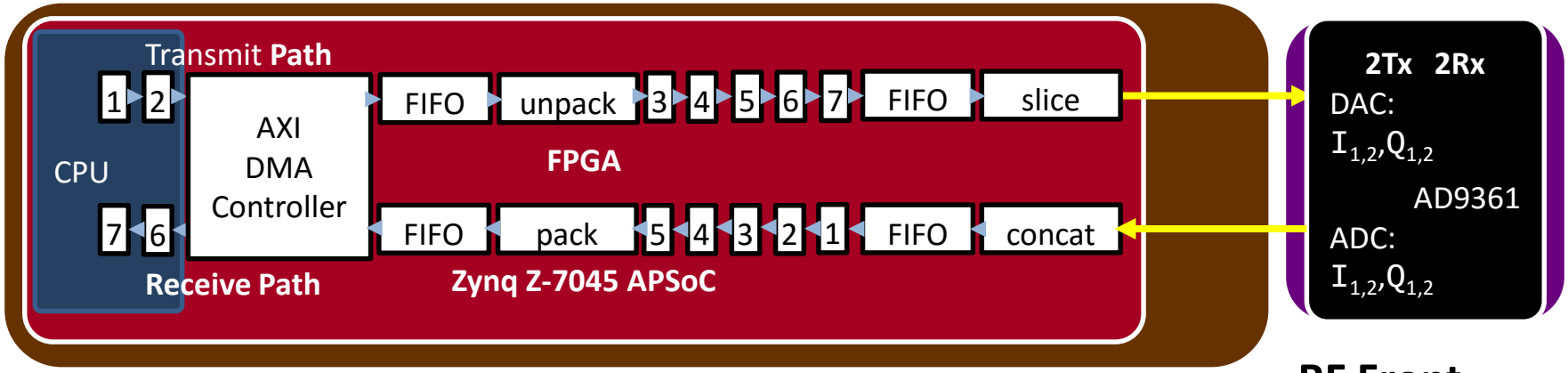
HW-SW Interfacing

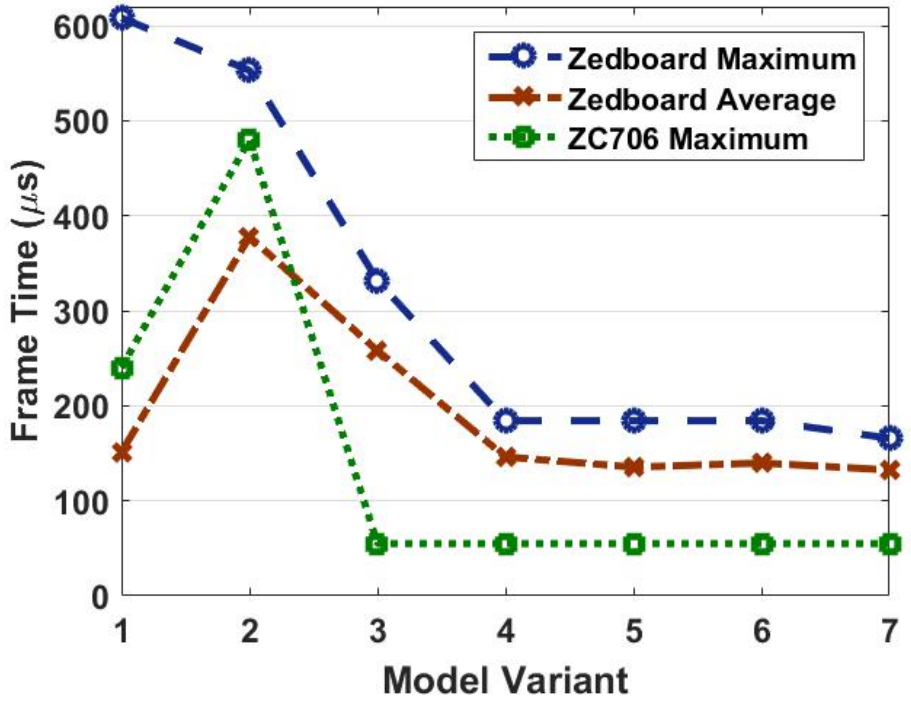


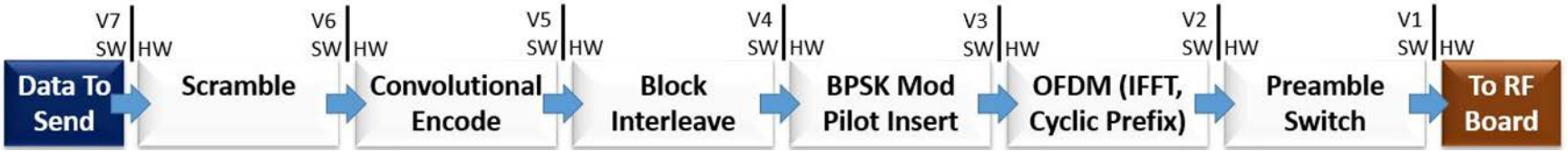
Heterogeneous Computing System

RF Front End:
ADI FMComms3

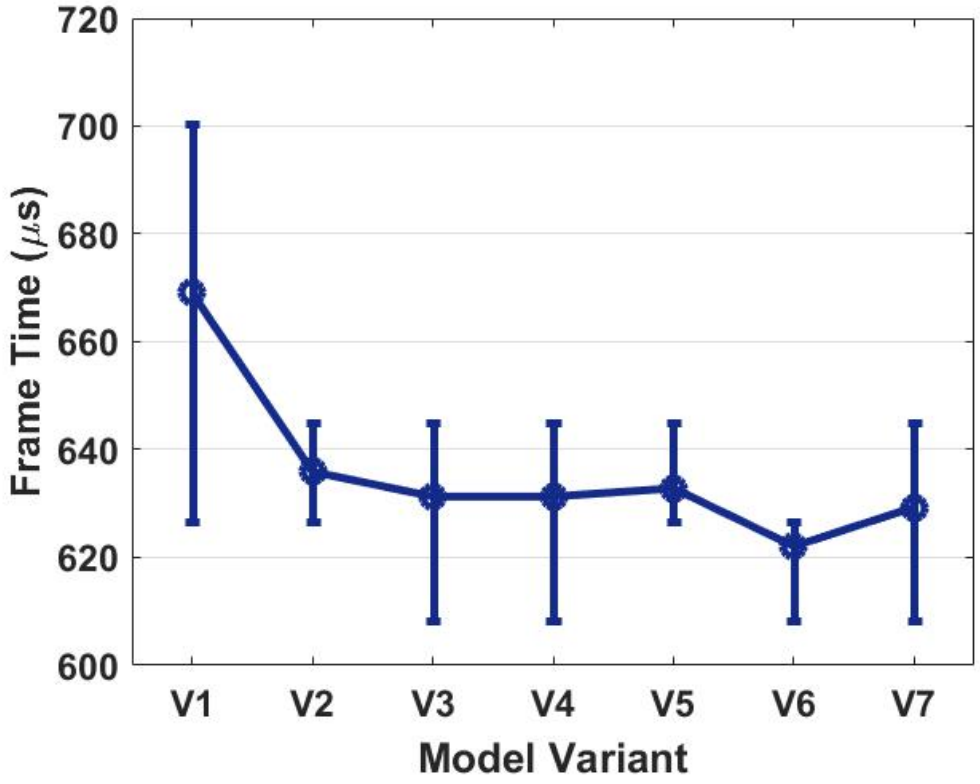
- DAC: Digital-to-Analog Converter
- **ADC: Analog-to-Digital Converter**
- **$I_{1(2)}$: In-Phase Channel 1 (or 2)**
- $Q_{1(2)}$: Quadrature Channel 1 (2)

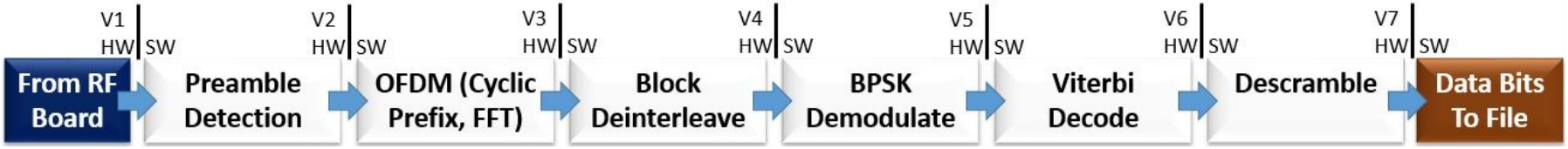
Transmitter frame times



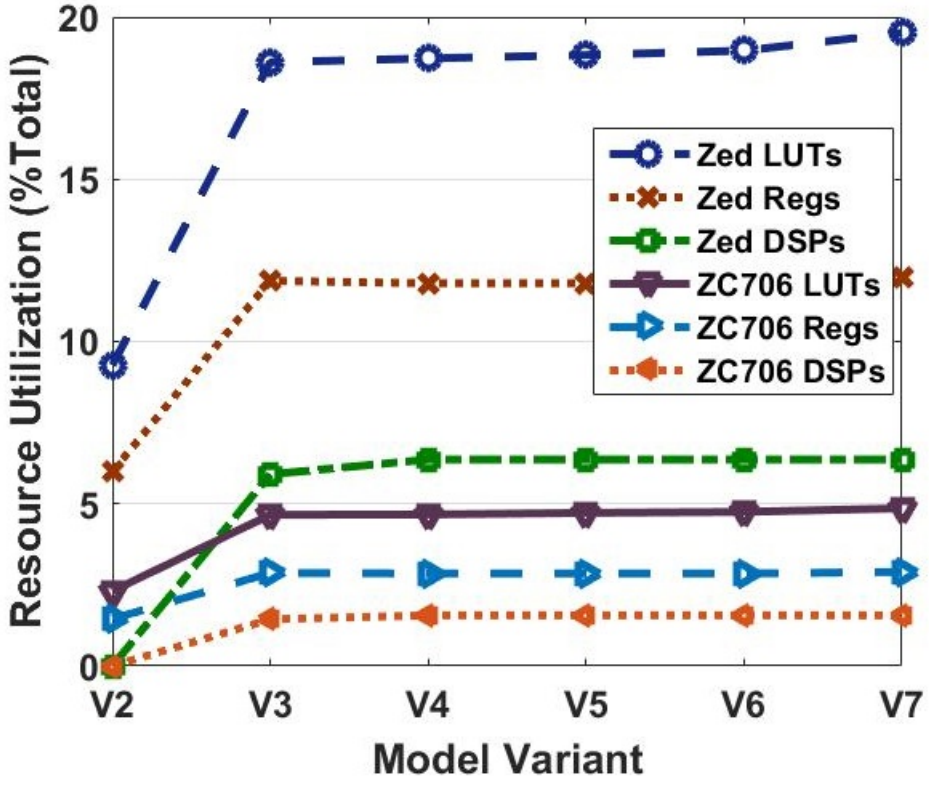


Receiver Frame times

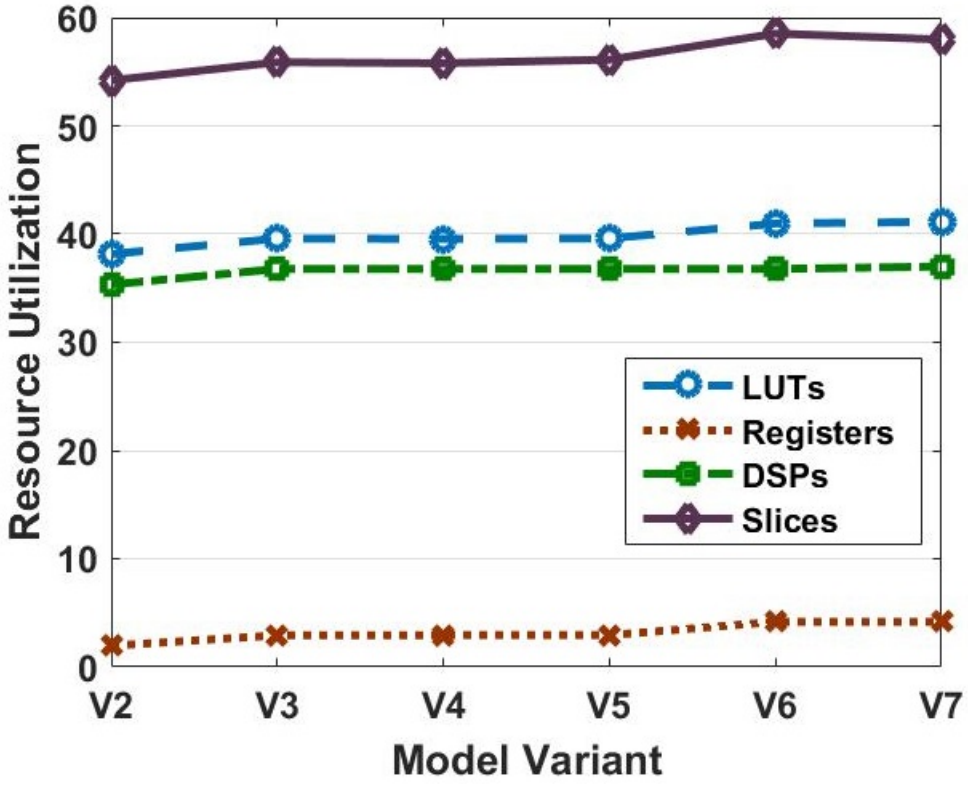




Transmit resource utilization



Receiver resource utilization



Energy consumption
Tx on Zedboard, Rx on ZC706

	Tx (mJ)	Rx (mJ)
PS	25.25	75.17
v2	30.01	112.46
v3	30.36	112.99
v4	30.44	101.33
v5	30.43	101.09
v6	30.48	101.33
v7	30.39	101.52

- From Vivado Power report

The Future

- Our framework will easily adapt/update to new hardware and capabilities
  - Xilinx Ultascale
  - Altera Arria
  - ADI has a new chip to replace the ADI 9361
- Co-existence of multiple standards on the same SOC:
  - 802.11
  - LTE
- Higher layers: MAC and PHY

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Reusability: Adapt to Modern Wireless Standards

Functional Unit	802.11 a	Wi-Fi (802.11g)	Mobile (LTE)
F1.Scrambling	X	X	X
F2.Convolutional Coding	X	X	X
F3.QPSK Modulation	X	V	X
F4.Block Interleaving	X	X	X
F5.Subcarrier Mapping	X	X	V
F6.OFDM	X	X	V
F7.Preamble Insertion	X	V	V

X: Equivalent, Reusable

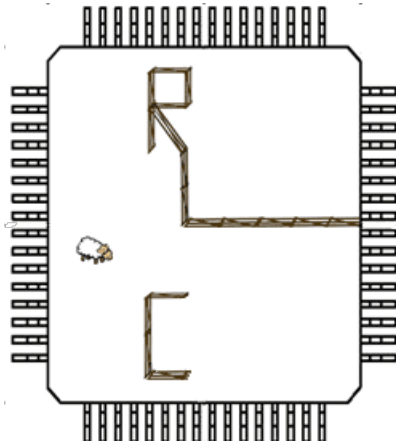
V: A Variant Can Be Reused

Generate HW and SW blocks

- SW: We use Mathworks Embedded Coder
- HW: Many choices:
  - Mathworks HDL coder
  - Xilinx System Generator
  - IP cores
  - …
- Automatically assign HW vs. SW?

Technology Keeps Improving

- Sheep auto-drafter:
  - The Sheep Auto Drafter is a fully automated weighing and drafting system that is smoother, quieter and easier to set up and operate than any other sheep drafting product on the market.



https://am.gallagher.com/nz/products/weighing-and-eid/drafters/G05714

Thank You!

- **Miriam Leeser: mel@coe.neu.edu**

  http://www.coe.neu.edu/Research/rcl/

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  - Mathworks
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  - Rahman Doost, Postdoc

- Current and Former Students
  - Benjamin Drozdenko
  - Jonathon Pendlum, Ettus Research
  - George Eichenger, MIT Lincoln Laboratory

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6th New England Workshop on Software Defined Radio

3 June 2016

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